











SLIS152B -MAY 2014-REVISED SEPTEMBER 2014

DRV5033

DRV5033 Digital-Omnipolar-Switch Hall Effect Sensor

1 Features

- Digital Omnipolar-Switch Hall Sensor
- · Superior Temperature Stability
 - B_{OP} ±10% Over Temperature
- High Sensitivity (B_{OP} and B_{RP})
 - ±6.9 / ±3.5 mT (AJ)
- · Detects North and South Magnetic Field
- · Supports a Wide Voltage Range
 - 2.5 to 38 V
 - No External Regulator Required
- Wide Operating Temperature Range
 - T_A = -40 to 125°C (Q, see Figure 22)
- Open Drain Output (30-mA Sink)
- Fast 35-µs Power-On Time
- Small Package and Footprint
 - Surface Mount 3-Pin SOT-23 (DBZ)
 - 2.92 mm × 2.37 mm
 - Through-Hole 3-Pin SIP (LPG)
 - $-4.00 \text{ mm} \times 3.15 \text{ mm}$

Protection Features

- Reverse Supply Protection (up to –22 V)
- Supports up to 40-V Load Dump
- Output Short-Circuit Protection
- Output Current Limitation

2 Applications

- · Docking Detection
- Door Open and Close Detection
- Proximity Sensing
- Valve Positioning
- · Pulse Counting

3 Description

The DRV5033 device is a chopper-stabilized Hall Effect Sensor that offers a magnetic sensing solution with superior sensitivity stability over temperature and integrated protection features.

The DRV5033 responds the same to both polarities of magnetic field direction. When the applied magnetic flux density exceeds the B_{OP} threshold, the DRV5033 open drain output goes low. The output stays low until the field decreases to less than B_{RP} , and then the output goes to high impedance. The output current sink capability is 30 mA. A wide operating voltage range from 2.5 V to 38 V with reverse polarity protection up to -22 V makes the device suitable for a wide range of industrial applications.

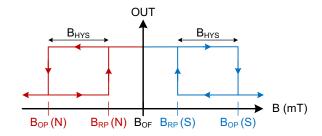
Internal protection functions are provided for reverse supply conditions, load dump, and output short circuit or over current.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)		
DD\/5022	SOT-23 (3)	2.92 mm × 2.37 mm		
DRV5033	SIP (3)	4.00 mm × 3.15 mm		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Output State



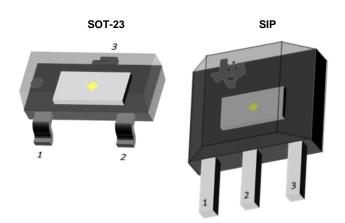




Table of Contents

1	Features 1	8 Detailed Description	8
2	Applications 1	8.1 Overview	8
3	Description 1	8.2 Functional Block Diagram	8
4	Output State 1	8.3 Feature Description	9
5	Revision History2	8.4 Device Functional Modes	14
6	Pin Configuration and Functions	9 Application and Implementation	15
7	Specifications	9.1 Application Information	15
•	7.1 Absolute Maximum Ratings	9.2 Typical Application	15
	7.2 Handling Ratings	10 Power Supply Recommendations	17
	7.3 Recommended Operating Conditions	11 Device and Documentation Support	18
	7.4 Thermal Information	11.1 Device Support	18
	7.5 Electrical Characteristics	11.2 Trademarks	19
	7.6 Switching Characteristics	11.3 Electrostatic Discharge Caution	19
	7.7 Magnetic Characteristics	11.4 Glossary	19
	7.8 Typical Characteristics 6	12 Mechanical, Packaging, and Orderable Information	19

5 Revision History

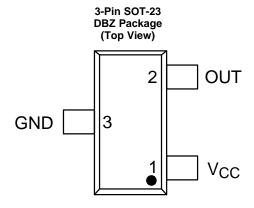
CI	changes from Revision A (August 2014) to Revision B	Page
•	Changed the maximum T _J value to 150°C	4
•	Added typical rise and fall time and removed maximum value in Switching Characteristics	!
•	Updated the Magnetic Characteristics values	{
•	Updated all Typical Characteristics graphs	(
•	Updated Equation 4	10

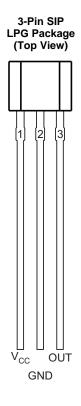
CI	hanges from Original (May 2014) to Revision A	Page
•	Changed High Sensitivity Options: +6.9 / +2.3 mT (AJ) to +6.9 / +3.5 mT (AJ)	1
•	Changed the maximum T _J value from 175°C to 150°C	4
•	Changed MIN value for I _{OCP} from 20 to 15	5
•	Changed Max value for I _{OCP} from 40 to 45	5
•	Updated Magnetic Characteristics table.	5



6 Pin Configuration and Functions

For additional configuration information, see *Device Markings* and *Mechanical, Packaging, and Orderable Information*.





Pin Functions

PIN				
NAME NUMBER DBZ LPG		TYPE	DESCRIPTION	
		LPG		
GND	ND 3 2		GND	Ground pin
OUT	2	3	Output	Hall sensor open-drain output. The open drain requires a resistor pullup.
V _{CC}	1	1	PWR	2.5 to 38 V power supply. Bypass this pin to the GND pin with a 0.01- μ F (minimum) ceramic capacitor rated for V _{CC} .

Product Folder Links: DRV5033



7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	V _{CC}	-22 ⁽²⁾	40	V
Power supply voltage	Voltage ramp rate (V _{CC}), V _{CC} < 5 V	Unlir	Unlimited	
	Voltage ramp rate (V _{CC}), V _{CC} > 5 V	0	2	V/µs
Output pin voltage	OUT	-0.5	40	V
Output pin reverse current during reverse supply condition	OUT	0	100	mA
Operating junction temperature	TJ	-40	150 ⁽³⁾	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T _{stg}	Storage tempe	rature range	-65	150	°C
V	Electrostatic	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	-2.5	2.5	kV
V _(ESD)	discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	-500	500	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Power supply voltage	2.5	38	V
Vo	Output pin voltage (OUT)	0	38	V
I _{SINK}	Output pin current sink (OUT) ⁽¹⁾	0	30	mA
T _A	Operating ambient temperature	-40	125	°C

⁽¹⁾ Power dissipation and thermal limits must be observed

7.4 Thermal Information

		DRV	DRV5033		
	THERMAL METRIC ⁽¹⁾	DBZ	LPG	UNIT	
		3 PINS	3 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	333.2	180		
R ₀ JC(top)	Junction-to-case (top) thermal resistance	99.9	98.6		
$R_{\theta JB}$	Junction-to-board thermal resistance	66.9	154.9	°C/W	
ΨЈТ	Junction-to-top characterization parameter	4.9	40		
ΨЈВ	Junction-to-board characterization parameter	65.2	154.9		

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

⁽²⁾ Ensured by design. Only tested to -20 V.

⁽³⁾ Tested in production to $T_A = 125$ °C.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER	SUPPLIES (V _{CC})					
V _{CC}	V _{CC} operating voltage		2.5		38	V
	Operating expels express	$V_{CC} = 2.5 \text{ to } 38 \text{ V}, T_A = 25^{\circ}\text{C}$		2.7		A
I _{CC}	Operating supply current	$V_{CC} = 2.5 \text{ to } 38 \text{ V}, T_A = 125^{\circ}\text{C}$		3	3.6 50	mA
t _{on}	Power-on time			35	50	μs
OPEN DE	RAIN OUTPUT (OUT)					
_	FET on-resistance	$V_{CC} = 3.3 \text{ V}, I_{O} = 10 \text{ mA}, T_{A} = 25^{\circ}\text{C}$		22		Ω
r _{DS(on)}	FET OII-TESISTATICE	$V_{CC} = 3.3 \text{ V}, I_{O} = 10 \text{ mA}, T_{A} = 125 ^{\circ}\text{C}$		36	50	12
I _{lkg(off)}	Off-state leakage current	Output Hi-Z			1	μΑ
PROTEC	TION CIRCUITS					
V_{CCR}	Reverse supply voltage		-22			V
I _{OCP}	Overcurrent protection level	OUT shorted V _{CC}	15	30	45	mA

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OPEN DR	OPEN DRAIN OUTPUT (OUT)						
t _d	Output delay time	$B = B_{RP} - 10 \text{ mT to } B_{OP} + 10 \text{ mT in } 1 \mu\text{s}$		13	25	μs	
t _r	Output rise time (10% to 90%)	R1 = 1 k Ω , C _O = 50 pF, V _{CC} = 3.3 V		200		ns	
t _f	Output fall time (90% to 10%)	R1 = 1 k Ω , C _O = 50 pF, V _{CC} = 3.3 V		31		ns	

7.7 Magnetic Characteristics

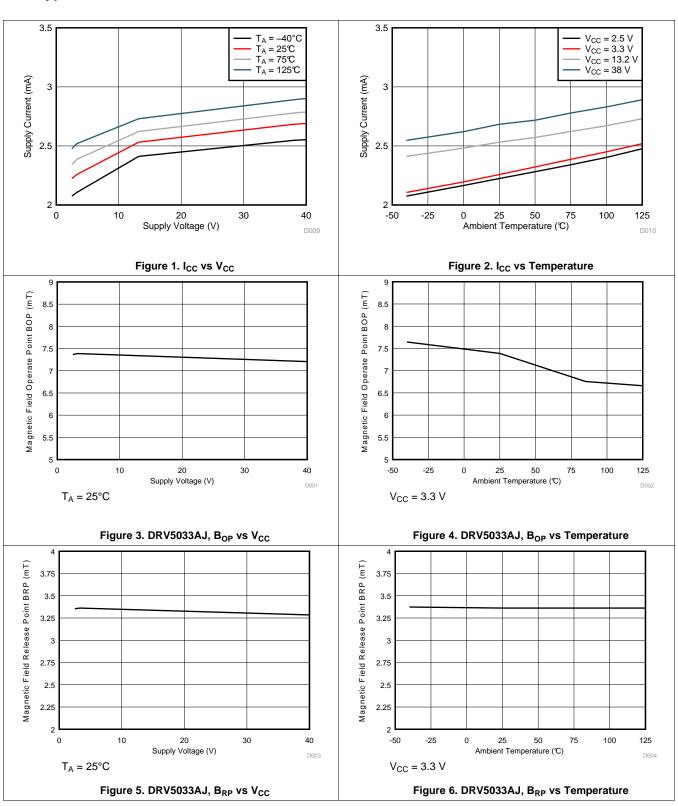
over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT ⁽¹⁾
f_{BW}	Bandwidth ⁽²⁾		20			kHz
DRV5033	AJ: ±6.9 / ±3.5 mT					
B _{OP}	Operate point; see Figure 12		±3	±6.9	±12	mT
B_RP	Release point; see Figure 12	$T_{\Delta} = -40^{\circ}\text{C} \text{ to } 125^{\circ}\text{C}$	±1	±3.5	±5	mT
B _{hys}	Hysteresis; $B_{hys} = (B_{OP} - B_{RP})^{(3)}$	1 _A = -40 C to 125 C		3.4		mT
B _O	Magnetic offset; $B_O = (B_{OP} + B_{RP}) / 2$		-	5.2		mT

- (1) 1 mT = 10 Gauss
- (2) Bandwidth describes the fastest changing magnetic field that can be detected and translated to the output.
- (3) $|B_{OP}|$ is always greater than $|B_{RP}|$.



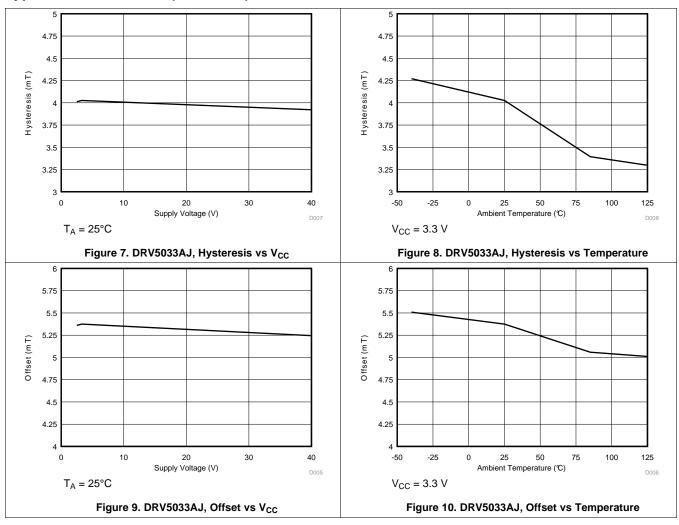
7.8 Typical Characteristics



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Typical Characteristics (continued)





8 Detailed Description

8.1 Overview

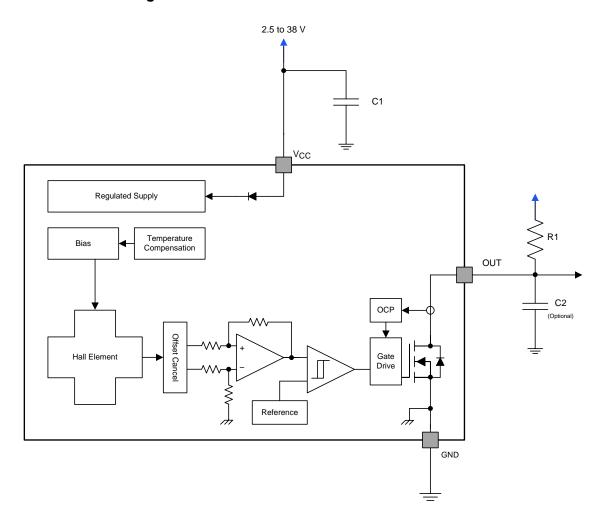
The DRV5033 device is a chopper-stabilized hall sensor with a digital omnipolar switch output for magnetic sensing applications. The DRV5033 device can be powered with a supply voltage between 2.5 and 38 V, and will survive -22 V reverse battery conditions continuously. Note that the DRV5033 device will not be operating when $-22 \sim 2.4$ V is applied to V_{CC} (with respect to GND). In addition, the device can withstand voltages up to 40 V for transient durations.

The field polarity is defined as follows: a south pole near the marked side of the package is a positive magnetic field. A north pole near the marked side of the package is a negative magnetic field.

The omnipolar configuration allows the hall sensor to respond to either a south or north pole. A strong magnetic field of either polarity will cause the output to pull low (operate point, B_{OP}), and a weaker magnetic field will cause the output to release (release point, B_{RP}). Hysteresis is included in between the operate and release points, so magnetic field noise will not trip the output accidentally.

An external pullup resistor is required on the OUT pin. The OUT pin can be pulled up to V_{CC} , or to a different voltage supply. This allows for easier interfacing with controller circuits.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Field Direction Definition

A positive magnetic field is defined as a south pole near the marked side of the package as shown in Figure 11.

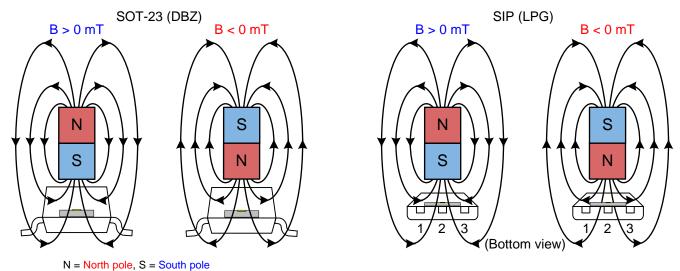


Figure 11. Field Direction Definition

8.3.2 Device Output

If the device is powered on with a magnetic field strength between B_{RP} and B_{OP} , then the device output is indeterminate and can either be Hi-Z or Low. If the field strength is greater than B_{OP} , then the output is pulled low. If the field strength is less than B_{RP} , then the output is released.

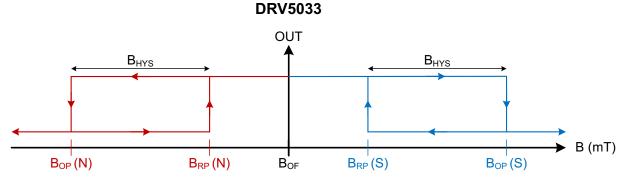


Figure 12. DRV5033— $B_{OP} > 0$



8.3.3 Power-On Time

After applying V_{CC} to the DRV5033 device, t_{on} must elapse before the OUT pin is valid. During the power-up sequence, the output is Hi-Z. A pulse as shown in Figure 13 and Figure 14 occurs at the end of t_{on} . This pulse can allow the host processor to determine when the DRV5033 output is valid after startup. In Case 1 (Figure 13) and Case 2 (Figure 14), the output is defined assuming a constant magnetic field B > B_{OP} and B < B_{RP}.

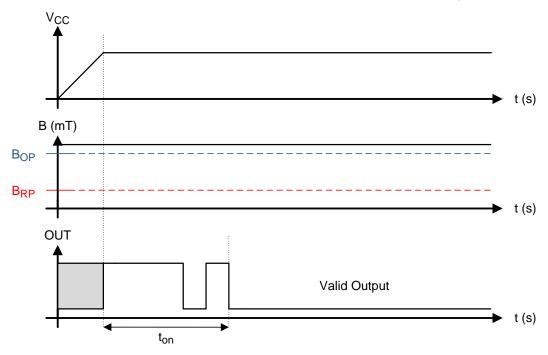


Figure 13. Case 1: Power On When $B > B_{OP}$

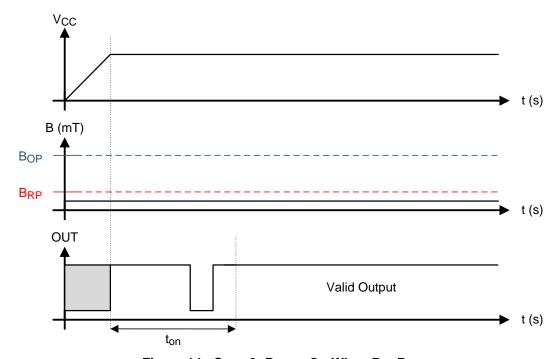


Figure 14. Case 2: Power On When $B < B_{RP}$

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If the device is powered on with the magnetic field strength $B_{RP} < B < B_{OP}$, then the device output is indeterminate and can either be Hi-Z or pulled low. During the power-up sequence, the output is held Hi-Z until t_{on} has elapsed. At the end of t_{on} , a pulse is given on the OUT pin to indicate that t_{on} has elapsed. After t_{on} , if the magnetic field changes such that $B_{OP} < B$, the output is released. Case 3 (Figure 15) and Case 4 (Figure 16) show examples of this behavior.

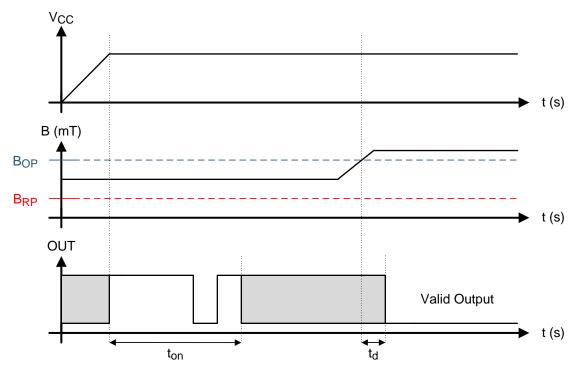


Figure 15. Case 3: Power On When $B_{RP} < B < B_{OP}$, Followed by $B > B_{OP}$



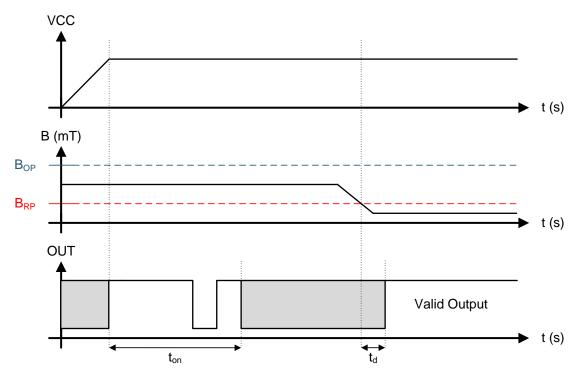


Figure 16. Case 4: Power On When $B_{RP} < B < B_{OP}$, Followed by $B < B_{RP}$

8.3.4 Output Stage

The DRV5033 output stage uses an open-drain NMOS, and it is rated to sink up to 30 mA of current. For proper operation, calculate the value of the pullup resistor R1 using Equation 1.

$$\frac{V_{ref} max}{30 mA} \le R1 \le \frac{V_{ref} min}{100 \mu A}$$
 (1)

The size of R1 is a tradeoff between the OUT rise time and the current when OUT is pulled low. A lower current is generally better, however faster transitions and bandwidth require a smaller resistor for faster switching.

In addition, ensure that the value of R1 > 500 Ω to ensure the output driver can pull the OUT pin close to GND.

NOTE

 V_{ref} is not restricted to V_{CC} . The allowable voltage range of this pin is specified in the *Absolute Maximum Ratings*.

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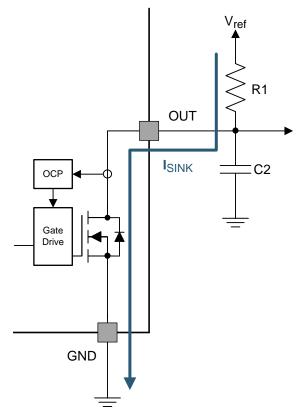


Figure 17.

Select a value for C2 based on the system bandwidth specifications as shown in Equation 2.

$$2 \times f_{\text{BW}} \text{ (Hz)} < \frac{1}{2\pi \times \text{R1} \times \text{C2}}$$

Most applications do no require this C2 filtering capacitor.

(2)



8.3.5 Protection Circuits

The DRV5033 device is fully protected against overcurrent and reverse-supply conditions.

8.3.5.1 Overcurrent Protection (OCP)

An analog current-limit circuit limits the current through the FET. The driver current is clamped to I_{OCP} . During this clamping, the $r_{DS(on)}$ of the output FET is increased from the nominal value.

8.3.5.2 Load Dump Protection

The DRV5033 device operates at DC V_{CC} conditions up to 38 V nominally, and can additionally withstand V_{CC} = 40 V. No current-limiting series resistor is required for this protection.

8.3.5.3 Reverse Supply Protection

The DRV5033 device is protected in the event that the V_{CC} pin and the GND pin are reversed (up to -22 V).

NOTE

In a reverse supply condition, the OUT pin reverse-current must not exceed the ratings specified in the *Absolute Maximum Ratings*.

FAULT	CONDITION	DEVICE	DESCRIPTION	RECOVERY	
FET overload (OCP)	I _{SINK} ≥ I _{OCP}	Operating	Output current is clamped to I _{OCP}	I _O < I _{OCP}	
Load dump	38 V < V _{CC} < 40 V	Operating	Device will operate for a transient duration	V _{CC} ≤ 38 V	
Reverse supply	leverse supply		Device will survive this condition	V _{CC} ≥ 2.5 V	

8.4 Device Functional Modes

The DRV5033 device is active only when V_{CC} is between 2.5 and 38 V.

When a reverse supply condition exists, the device is inactive.



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV5033 device is used in magnetic-field sensing applications.

9.2 Typical Application

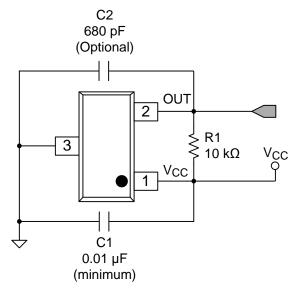


Figure 18. Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE		
Supply voltage	V _{CC}	3.2 to 3.4 V		
System bandwidth	f_{BW}	10 kHz		

9.2.2 Detailed Design Procedure

Table 2. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C1	V _{CC}	GND	A 0.01-μF (minimum) ceramic capacitor rated for V _{CC}
C2	OUT	GND	Optional: Place a ceramic capacitor to GND
R1	OUT	REF ⁽¹⁾	Requires a resistor pullup

(1) REF is not a pin on the DRV5033 device, but a REF supply-voltage pullup is required for the OUT pin; the OUT pin may be pulled up to V_{CC}.



9.2.2.1 Configuration Example

In a 3.3-V system, 3.2 V \leq V_{ref} \leq 3.4 V. Use Equation 3 to calculate the allowable range for R1.

$$\frac{V_{ref} max}{30 mA} \le R1 \le \frac{V_{ref} min}{100 \mu A}$$
(3)

For this design example, use Equation 4 to calculate the allowable range of R1.

$$\frac{3.4 \text{ V}}{30 \text{ mA}} \le \text{R1} \le \frac{3.2 \text{ V}}{100 \text{ \muA}}$$
 (4)

Therefore:

$$113 \Omega \le R1 \le 32 k\Omega \tag{5}$$

After finding the allowable range of R1 (Equation 5), select a value between 500 Ω and 32 k Ω for R1.

Assuming a system bandwidth of 10 kHz, use Equation 6 to calculate the value of C2.

$$2 \times f_{\text{BW}} \text{ (Hz)} < \frac{1}{2\pi \times \text{R1} \times \text{C2}}$$
 (6)

For this design example, use Equation 7 to calculate the value of C2.

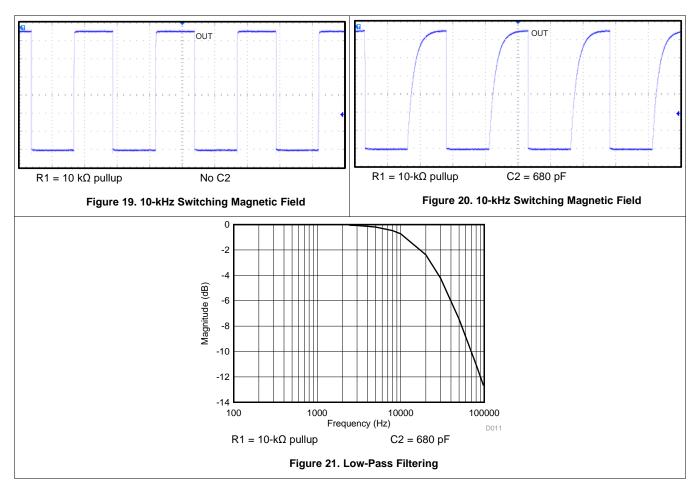
$$2 \times 10 \text{ kHz} < \frac{1}{2\pi \times R1 \times C2} \tag{7}$$

An R1 value of 10 k Ω and a C2 value less than 820 pF satisfy the requirement for a 10-kHz system bandwidth. A selection of R1 = 10 k Ω and C2 = 680 pF would cause a low-pass filter with a corner frequency of 23.4 kHz.

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9.2.3 Application Curves



10 Power Supply Recommendations

The DRV5033 device is designed to operate from an input voltage supply (VM) range between 2.5 and 38 V. A 0.01- μ F (minimum) ceramic capacitor rated for V_{CC} must be placed as close to the DRV5033 device as possible.



11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Figure 22 shows a legend for reading the complete device name for and DRV5033 device.

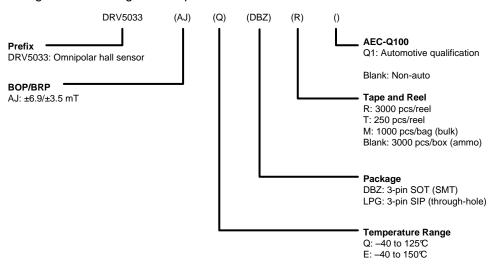


Figure 22. Device Nomenclature

11.1.2 Device Markings

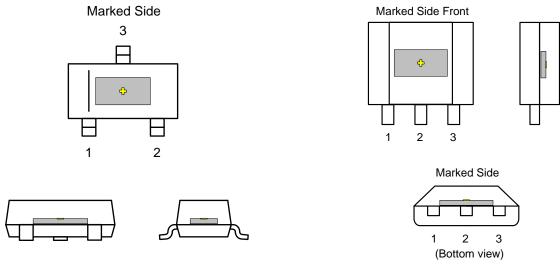


Figure 23. SOT-23 (DBZ) Package

Figure 24. SIP (LPG) Package

• indicates the Hall effect sensor (not to scale). The Hall element is located in the center of the package with a tolerance of ±100 μm. The height of the Hall element from the bottom of the package is 0.7 mm ±50 μm in the DBZ package and 0.987 mm ±50 μm in the LPG package.



11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.





18-Sep-2014

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
DRV5033AJQDBZR	PREVIEW	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+QLAJ	
DRV5033AJQLPG	PREVIEW	TO-92	LPG	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	+QLAJ	
PDRV5033AJQDBZT	PREVIEW	SOT-23	DBZ	3	250	TBD	Call TI	Call TI	-40 to 125		
PDRV5033AJQLPG	PREVIEW	TO-92	LPG	3	2000	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

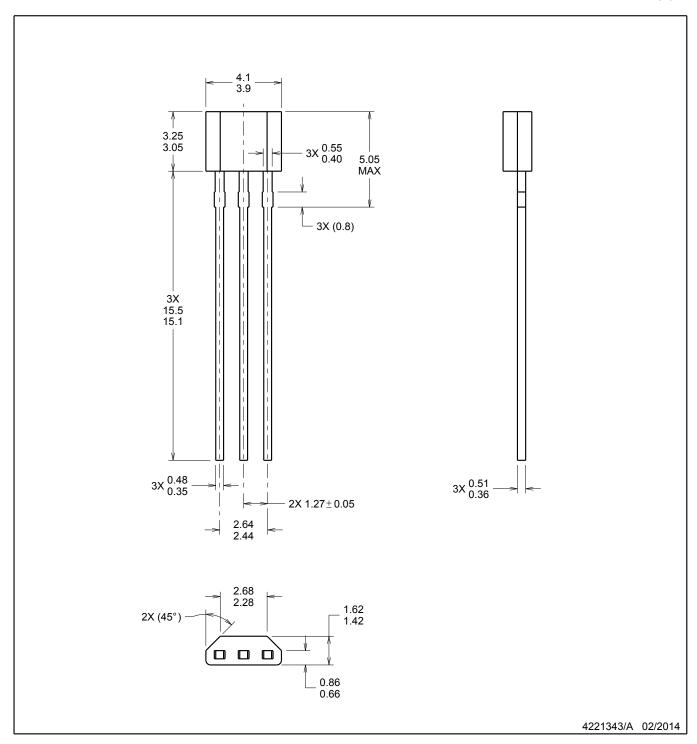
18-Sep-2014

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TO-92



NOTES:

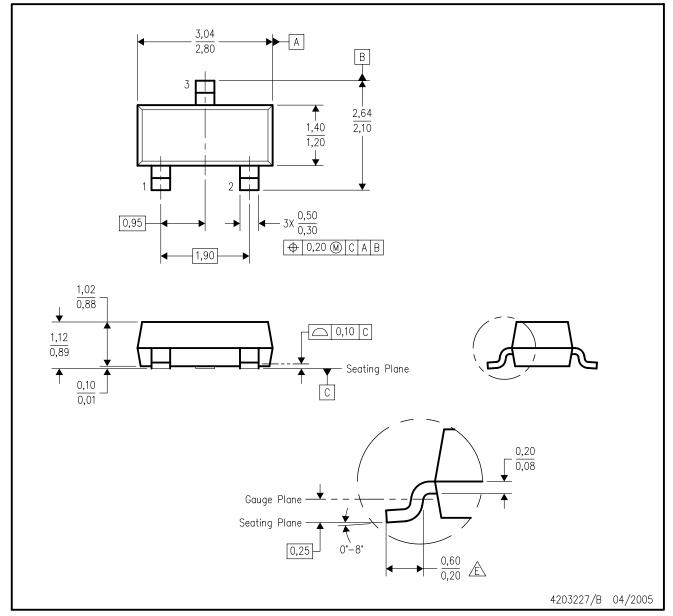
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.



DBZ (R-PDSO-G3)

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Lead dimensions are inclusive of plating.
- D. Body dimensions are exclusive of mold flash and protrusion. Mold flash and protrusion not to exceed 0.25 per side.
- Falls within JEDEC TO-236 variation AB, except minimum foot length.



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